

cell;

a number of wordlines coupled to the gate region of at least one memory cell;

[at least one] a strapping line of lower resistance than the wordlines coupled to [at least one of the number of wordlines] a single wordline wherein the strapping line bypasses a portion of the single wordline, and wherein the strapping line is spaced apart from adjacent conductive structures by a distance greater than a wordline pitch; and

at least two channels connecting the strapping line to a first and second end of the portion of the single wordline.

8. (Amended) A memory device, comprising:

a number of memory cells having a first source/drain region and a second source/drain region and a gate region;

a number of source lines coupled to the first source/drain region of at least one memory cell;

a number of bit lines coupled to the second source/drain region of at least one memory cell;

an array of parallel wordlines coupled to the gate region of at least one memory cell, the array of parallel wordlines having a pitch;

a number of strapping devices which bypass portions of the wordlines in the array of parallel wordlines, each strapping device comprising:

a strapping line of lower resistance than the wordlines, wherein the strapping lines are each located a distance from each other that is greater than the pitch; and

at least two channels connecting [the] each strapping line to [the] a portion of a single wordline.

15. (Amended) An integrated circuit comprising:

at least one memory array comprising:

a number of memory cells having a first source/drain region and a second source/drain region and a gate region;

a number of source lines coupled to the first source/drain region of at least one memory cell;

a number of bit lines coupled to the second source/drain region of at least one memory cell;

a number of wordlines coupled to the gate region of at least one memory cell;

[at least one] a strapping line of lower resistance than the wordlines coupled to [at least one of the number of wordlines] a single wordline wherein the strapping line bypasses a portion of the single wordline, and wherein the strapping line is spaced apart from adjacent conductive structures by a distance greater than a wordline pitch;

at least two channels connecting the strapping line to a first and second end of the portion of the single wordline;

a row decoder;

a column decoder; and

a sense amplifier.

19. (Amended) An integrated circuit comprising:

at least one memory array comprising:

a number of memory cells having a first source/drain region and a second source/drain region and a gate region;

a number of source lines coupled to the first source/drain region of at least one memory cell;

a number of bit lines coupled to the second source/drain region of at least one memory cell;

an array of parallel wordlines coupled to the gate region of at least one memory cell, the array of parallel wordlines having a pitch;

a number of strapping devices which bypass [portions of the] a portion of single wordlines in the array of parallel wordlines, each strapping device comprising:

a strapping line of lower resistance than the wordlines, wherein the strapping lines are each located a distance from each other that is greater than the pitch;

- at least two channels connecting the strapping line to the single wordline;
 - a row decoder;
 - a column decoder; and
 - a sense amplifier.
26. (Amended) An information handling device comprising:
- a processing unit;
 - at least one memory array comprising:
 - a number of memory cells having a first source/drain region and a second source/drain region and a gate region;
 - a number of source lines coupled to the first source/drain region of at least one memory cell;
 - a number of bit lines coupled to the second source/drain region of at least one memory cell;
 - a number of wordlines coupled to the gate region of at least one memory cell;
 - [at least one] a strapping line of lower resistance than the wordlines coupled to [at least one of the number of wordlines] a single wordline wherein the strapping line bypasses a portion of the single wordline, and wherein the strapping line is spaced apart from adjacent conductive structures by a distance greater than a wordline pitch;
 - at least two channels connecting the strapping line to the single wordline; and
 - a system bus connecting the processing unit to the memory array.
30. (Amended) An information handling device comprising:
- a processing unit;
 - at least one memory array comprising:
 - a number of memory cells having a first source/drain region and a second source/drain region and a gate region;
 - a number of source lines coupled to the first source/drain region of at least one memory cell;

a number of bit lines coupled to the second source/drain region of at least one memory cell;

an array of parallel wordlines coupled to the gate region of at least one memory cell, the array of parallel wordlines having a pitch;

a number of strapping devices which bypass portions of the wordlines in the array of parallel wordlines, each strapping device comprising:

a strapping line of lower resistance than the wordlines, wherein the strapping lines are each located a distance from each other that is greater than the pitch;

at least two channels connecting [the] each strapping line to [the wordline] single wordlines; and

a system bus connecting the processing unit to the memory array.

37. (Amended) A method of reducing a wordline RC time constant comprising:

[activating a selected row in a memory array, comprising:]

spacing a number of strapping devices over wordlines in a memory array apart from adjacent strapping devices by a distance greater than a wordline pitch;

connecting individual strapping devices to portions of single wordlines using at least two channels for each strapping device;

activating a first number of transistors coupled to a first portion of a wordline; and
activating a second number of transistors coupled to a second portion of a wordline, wherein a signal used for activating the second number of transistors bypasses the first portion of the wordline through a strapping device of lower resistance than the first portion of the wordline;

activating a selected bitline in the memory array associated with a selected memory cell;
discharging the selected memory cell through a selected transistor, the selected transistor being activated by both the selected row and the selected bitline; and

sensing the presence or absence of a charge from the selected memory cell through the use of a sense amplifier.

42. (Amended) A method of reducing a wordline RC time constant in a memory bank comprising:

activating a plurality of selected coupled wordlines in a plurality of memory arrays, comprising:

activating a first wordline in a first memory array; and

activating a second wordline in a second memory array, wherein a signal used for activating the second wordline bypasses the first wordline through a strapping device of lower resistance than the first wordline, wherein the strapping device is spaced apart from adjacent strapping devices by a spacing greater than a wordline pitch, and wherein the strapping device is connected to the coupled wordlines by at least two channels;

activating a selected bitline in one of the plurality of memory arrays associated with a selected memory cell;

discharging the selected memory cell through a selected transistor, the selected transistor being activated by both the plurality of selected coupled wordlines and the selected bitline; and sensing the presence or absence of a charge from the selected memory cell through the use of a sense amplifier.

43. (Amended) The method of reducing a wordline RC time constant of claim [37] 42, wherein activating a second wordline in a second memory array comprises:

sending a signal through a first channel to a metal strapping line;

sending the signal through the metal strapping line; and

sending the signal through a second channel to the second wordline.

45. (Amended) A method of forming a memory device comprising:

forming a number of memory cells having a first source/drain region and a second source/drain region and a gate region;

coupling a number of source lines to the first source/drain region of at least one memory cell;

coupling a number of bit lines to the second source/drain region of at least one memory

cell;

attaching a number of wordlines to the gate region of at least one memory cell;

attaching [at least one] a strapping line of lower resistance than the wordlines to [at least one of the number of wordlines] a single wordline wherein the strapping line bypasses a portion of the single wordline, wherein the strapping line is spaced apart from adjacent conductive structures by a spacing greater than a wordline pitch; and

connecting the strapping line to the single wordline by forming at least two channels from the strapping line to the single wordline.

49. (Amended) A method of forming a memory device comprising:

forming a number of memory cells having a first source/drain region and a second source/drain region and a gate region;

coupling a number of source lines coupled to the first source/drain region of at least one memory cell;

coupling a number of bit lines coupled to the second source/drain region of at least one memory cell;

attaching an array of parallel wordlines to the gate region of at least one memory cell, the array of parallel wordlines having a pitch;

attaching a number of strapping lines of lower resistance than the wordlines which bypass portions of the wordlines in the array of parallel wordlines, wherein the strapping lines are each located a distance from each other that is greater than the pitch; and

connecting the strapping lines to the wordlines by forming at least two channels from each strapping line to [the wordline] individual wordlines.